


**DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE
(AUTONOMOUS)**

(Approved by AICTE & Affiliated to Anna University, Chennai)
Re-Accredited by NAAC with 'A' Grade
Accredited by NBA for AERO, BME, CSE, ECE, EEE, IT & MECH.

PERAMBALUR-621212, TAMILNADU, INDIA.
Website: www.dsengg.ac.in


COURSE PLAN (2025-2026) ODD SEM

Name of the Faculty				
Designation/Department	ASSISTANT PROFESSOR / ECE			
Course Code/Name	U23ECT31 / DIGITAL SYSTEM DESIGN			
Year/Section/Department	II / III / ECE - C			
Credits Details	L: 3	T: 0	P: 0	C: 3
Total Contact Hours Required	45			

Syllabus:

UNIT I / NUMBER SYSTEMS AND CODE CONVERSIONS	09
Review of number systems-representation-conversions, Review of Boolean algebra- theorems, sum of product and product of sum simplification, canonical forms min term and max term, Simplification of Boolean expressions-Karnaugh map, Implementation of Boolean expressions using universal gates, Tabulation methods.	
UNIT II / COMBINATIONAL LOGIC CIRCUIT AND DESIGN	09
Problem formulation and design of combinational circuits - Code-Converters, Half and Full Adders, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Magnitude Comparator, Decoder, Encoder, Priority Encoder, Mux/Demux, Case study: Parity Generator/Checker, Seven Segment display decoder	
UNIT III/ SYNCHRONOUS SEQUENTIAL CIRCUITS	09
Latches, Flip flops – SR, JK, T, D, Master/Slave FF, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, lock - out condition circuit implementation - Counters, Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.	
UNIT IV/ ASYNCHRONOUS SEQUENTIAL LOGIC CIRCUITS	09
Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.	
UNIT V/ MEMORY AND PROGRAMMABLE LOGIC	09
RAM and ROM – Memory Decoding – Error Detection and Correction – Programmable Logic Array – Programmable Array Logic – Sequential Programmable Devices – Application Specific Integrated Circuits.	

Objective:

- ❖ To present the fundamentals of digital circuits and simplification methods.
- ❖ To practice the design of various combinational digital circuits using logic gates
- ❖ To bring out the analysis and design procedures for synchronous and asynchronous Sequential circuits.
- ❖ To learn integrated circuit families
- ❖ To introduce semiconductor memories and related technology

Text Book:

- T1:** M.Morris Mano, Michael D Ciletti, "Digital Design" 4th edition Pearson, 2011.
T2: Thomas L.Floyd, "Digital Fundamentals", Prentice Hall, 11th Edition, 2015.
T3: Floyd and Jain, "Digital Fundamentals", Pearsons Publication, 10th Edition, 2015

Reference Book:

- R1:** Anand Kumar, "Fundamentals of Digital Circuits", 4th Edition PHI Learning Private Limited, 2016.
R2: Donald P Leach, Albert Paul Malvino and Goutam Saha, "Digital Principles and Applications", 6th edition, Tata McGraw Hill Publishing Company Ltd, New Delhi,2008
R3: Tocci R J, "Digital systems: Principles and Applications", PHI learning, New Delhi, 10th Edition, 2006.
R4: Charles H. Roth, Larry L. Kinney "Fundamentals of Logic Design", Cengage Learning, 2015.
R5: R.P.Jain, "Modern Digital Electronics", 4thEdition, Tata McGraw-Hill Education, 2009.

Website:

- W1. nptel.ac.in/courses/117106086/26
W2. <https://nptel.ac.in/courses/117/106/117106086/>
W3. www.brainkart.com/.../Design-Procedure-of-Asynchronous-Sequential-circuits_6766/
W4. <https://www.youtube.com/watch?v=wyFSjAMdIvQ>
W5. <https://youtube/CLUoWkJUnN0>
W6. nptel.ac.in/video.php?subjectId=117106086
W7. <https://www.youtube.com/watch?v=x1NK8WQC3Z0>

Online Mode of Study:

- ❖ NPTEL: <https://freevideolectures.com/course/3164/digital-electronics>
- ❖ Class central: <https://www.classcentral.com/course/swayam-digital-electronic-circuits-12953>
- ❖ Udemy: <https://www.udemy.com/course/digital-electronics-logic-design/>
- ❖ edx: <https://www.edx.org/course/computations-structures-part-1-digital-circuits>
- ❖ coursera: <https://www.coursera.org/learn/digital-systems>

Course Plan:

Topic Number	Topic	Reference Detail	Page Number	Mode of teaching	Number of Periods Required	Cumulative Period
UNIT I - NUMBER SYSTEMS AND CODE CONVERSIONS (09)						
1	Review of number systems, representation, conversions	T1	1-30	BB	1	1
2	Review of Boolean algebra-theorems	T1	38-43	BB	1	2
3	sum of product and product of sum simplification	T1	43-50	BB	1	3
4	canonical forms min term and max term	T1	51-58	BB	1	4
5	Simplification of Boolean expressions-Karnaugh map	T1	73-88	BB	2	6
6	Implementation of Boolean expressions using universal gates	T1	90-97	BB	1	7
7	Tabulation methods	R4	159-181	BB	2	9
Outcome of Unit I:						
Use Boolean algebra and simplification procedures relevant to digital logic.						
UNIT II - COMBINATIONAL LOGIC CIRCUIT AND DESIGN (09)						
8	Problem formulation and design of combinational circuits	T1	125-129	BB	1	10
9	Code-Converters	R4	514-518	BB	1	11
10	Half and Full Adders, Binary Parallel Adder	T3	173-177	BB	1	12
11	Carry look ahead Adder, BCD Adder	T3	185-187	BB	1	13
12	Magnitude Comparator	T3	190-192	BB	1	14
13	Decoder, Encoder, Priority Encoder	T1	150-155	BB	1	15
14	Multiplexer and demultiplexer.	T1	155-158	BB	1	16
15	Case study: Parity Generator/Checker	T2	125-127	BB	1	17

16	Seven Segment display decoder	T3	235-238	BB	1	18
Outcome of Unit II:						
Design various combinational digital circuits using logic gates.						
UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS (09)						
17	Latches, Flip flops – SR, JK, T, D	T1	190-193	BB	2	20
18	Master Slave Flipflops, Triggering of FF	T1	193-196	BB	1	21
19	Analysis and design of clocked sequential circuits	T1	197-204	BB	1	22
20	Moore/Mealy models	R4	406-408	BB	1	23
21	state minimization, state assignment, lock - out condition circuit implementation	R4	474-495	BB	1	24
22	Counters, Ripple Counters, Ring Counters	T1	266-278	BB	2	26
23	Shift registers, Universal Shift Register.	T1	255-258	BB	1	27
Outcome of Unit III:						
Analyse and design synchronous sequential circuits.						
UNIT IV - ASYNCHRONOUS SEQUENTIAL LOGIC (09)						
24	Stable and Unstable states	W3	-	PPT	1	28
25	Output specifications	W3	-	PPT	1	29
26	Cycles and races	R1	551-552	BB	1	30
27	State reduction	T3	233-237	BB	2	32
28	Race free assignments	T3	464-468	BB	1	33
29	Hazards, Essential Hazards	T3	469-479	BB	1	34
30	Fundamental and Pulse mode sequential circuits	T2	534-549	BB	1	35
31	Design of Hazard free circuits	T3	474-480	BB	1	36
Outcome of Unit IV:						
CO4: Analyse and design asynchronous sequential circuits						

UNIT V - MEMORY AND PROGRAMMABLE LOGIC (09)

32	RAM and ROM	T1	300-306	PPT	1	37
33	Memory Decoding	T1	307-312	PPT	1	38
34	Error Detection and Correction	T1	312-315	PPT	1	39
35	Programmable Logic Array	T1	321-325	BB	2	41
36	Programmable Array Logic	T1	325-329	BB	2	43
37	Sequential Programmable Devices	T1	462-468	PPT	1	44
38	Application Specific Integrated Circuits.	T3	351-352	PPT	1	45

Outcome of Unit V:

C05: Build logic gates and use programmable devices.

C06: Understand the concepts of memory devices.

Course Outcome:

At the end of course: Students should be able to:

C01: Use Boolean algebra and simplification procedures relevant to digital logic.

C02: Design various combinational digital circuits using logic gates.

C03: Analyse and design synchronous sequential circuits

C04: Analyse and design asynchronous sequential circuits.

C05: Build logic gates and use programmable devices.

C06: Understand the concepts of memory devices

Course Outcome Vs Program Outcome Mapping:

COs	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	P012	PS01	PS02
C01	3	2	1	1	2	-	-	-	-	1	1	1	2	2
C02	3	2	1	1	-	-	-	-	-	-	1	1	3	3
C03	3	2	1	3	1	-	-	-	-	-	-	1	2	3
C04	2	2	1	-	-	-	-	-	-	1	1	1	3	2
C05	3	2	-	2	-	-	-	-	-	-	1	-	2	2
C06	3	2	1	1	1	-	-	-	-	1	1	1	2	2
AVG	2.8	2	1	1.6	1.3	-	-	-	-	1	1	1	2.3	2.3

Content beyond Syllabus:

- ❖ Finite State Machine
- ❖ CMOS Logic families

Internal Evaluation Components:

Webportal	Assignment	Components	Topic Number with Topic / Unit Details	Relevance to CO
Webportal 1	--	Assessment - I (60)	Unit I and II	CO 1 & CO2
	1	Assignment - Handwritten (20)	5.Simplification of Boolean expressions-Karnaugh map 10.Half and Full Adders, Binary Parallel Adder	CO 1 CO2
	2	Assignment - Poster Presentation / PPT (20)	1.Review of number systems, representation, conversions 16.Seven Segment display decoder	CO 1 CO2
Webportal 2	--	Assessment - II (60)	Unit III and IV	CO3 & CO4
	3	Seminar (20)	22.Counters, Ripple Counters, Ring Counters 29.Hazards, Essential Hazards	CO3 CO4
	4	Case Study Report (20)	20.Moore/Mealy models 30.Fundamental and Pulse mode sequential circuits	CO3 CO4
Webportal 3	--	Model Exam (75)	Unit I to V	CO1 to CO6
	5	MCQ (15)	Unit I to V	CO1 to CO6
	-	Course Attendance (10)	--	--

***Note:**

- ❖ Seminar contents should be of minimum 8 pages.
- ❖ PPT contents should be of minimum 24 slides.
- ❖ Each students Seminar and PPT should not be in Unique.

Submission Details:

Phase1(BeforeAT1)	Phase2(BeforeAT2)	Phase3(BeforeAT3)
Assignment 1	Assignment 2	Assignment 3

Google Class Code Details:

Class Link: <https://classroom.google.com/c/NzkwMDUzMTgzMjgy?cjc=mfuweufe>

Class Code: mfuweufe

PLAN OF ASSESSMENT TEST -DISTRIBUTION OF MARKS:

TEST	CO- MARK WISE DISTRIBUTION						BLOOM'S LEVEL MARK WISE DISTRIBUTION					
	CO1	CO2	CO3	CO4	CO5	CO6	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6
AT-1												
AT-2												
MODEL												

Prepared By

Verified By

(HOD/ECE)

Approved By

(PRINCIPAL)